Application Hints

Fault-tolerant CAN Transceiver

PCA82C252 / TJA1053 / TJA1054 / TJA1054A

Version 3.1

Date : 23rd of November 2001

Philips Semiconductors

PHILIPS

Revision History

Changes Version 1.0 -> 2.0 :

1. Chapter 3, calculation examples for PCA82C252 and TJA1053 added, new aspects
2. Chapter 4, calculation hints for termination resistors added, new aspects

Changes Version 2.0 -> 2.1 :

1. Chapter 6 added
2. Chapter 7 added
3. Chapter 8 added

Changes Version 2.1 -> 2.2 :

1. Chapter 5, clarification that external ESD diodes are optional for further improvements
2. Chapter 8 added, Software design hints (previous chapter 8 re-numbered to chapter 9)
3. Chapter 9, FAQ 9.6, No communication at CANH to VCC short circuit

Changes Version 2.2 -> 3.0 :

1. Foreword added
2. Chapter 2 added, Upgrading Note TJA1053 -> TJA1054
3. Chapter 3 added, Mode Control of the TJA1054
4. Chapter 5, formula 11 corrected, calculation example updated
5. Chapter 10, Software design hints dealing with the pin ERR added

Changes Version 3.0 -> 3.1 :

1. Editorial changes
2. Chapter 8, series resistor at pin WAKE, more details
3. Chapter 9 added, series resistor at pins TXD

Foreword

In this document, application related information for the various fault-tolerant transceiver implementations from Philips Semiconductors is collected. The different transceivers are a result of a continuous improvement of the fault-tolerant and system performance.
The first available product in the market was the PCA82C252, followed by the TJA1053 and later on by the TJA1054. In the mean time even the TJA1054 has become improved with respect to ESD capabilities. The so-called TJA1054**A** behaves identical to the TJA1054 but offers a higher ESD robustness on the bus-related pins. Thus wherever the TJA1054 is mentioned within this document it could also be read as TJA1054A, except in case a certain transceiver type is mentioned explicitly.

Table of Contents :

1. Comparison PCA82C252 / TJA1053 / TJA1054 / TJA1054A

1.1. System parameters

Key	PCA82C252	TJA1053	TJA1054
System size	10 – 15 nodes [1) 2)]	10 – 15 nodes [2)]	> 32 nodes
Speed	20 - <125 kbps [3)]	20 – 125 kbps	40 – 125 kbps
Emission	+	+	++
Immunity	+	+	++
TxD dominant monitoring	no	yes	yes
Extended bus failure management (CANH to Vcc)	no	no	yes
Resolved problem of arbitration across open failures	no	yes	yes

1) The limit is given by the performance during CANH to ground failures, which very much depends on the size and type of cable used.
2) The limit is given by the wake-up capability during CANH to ground failures, which very much depends on the values of the distributed terminations across the network. Therefore, exact figures of system size cannot be given.
3) With CANH to VBAT failures the delay of the dominant edge is increased. The maximum speed strongly depends on the inductance of the cable used.

1.2. Device parameters

Key	PCA82C252	TJA1053	TJA1054	TJA1054A
Current consumption in Normal Mode (I_{CC})	6 mA (rec) 29 mA (dom)	6 mA (rec) 29 mA (dom)	7 mA (rec) 17 mA (dom)	7 mA (rec) 17 mA (dom)
Current consumption in Standby Modes (I_{BAT} + I_{CC})	70 uA	70 uA	30 uA	30 uA
Minimum operating voltage	6V	6V	5V	5V
Prevention of VBAT reverse current [1)]	no	no	yes	yes
WAKE sensitivity	negative edge	negative edge	both edges	both edges
Vcc Standby mode	yes	yes	no	no
ERR reporting of open failures	during frame only	during frame only	during frame and inter frame space	during frame and inter frame space
ESD Protection pins RTH / RTL / CANH / CANL	2kV Human Body 200V Machine M.	2kV Human Body 200V Machine M.	2kV Human Body 200V Machine M.	4kV Human Body 300V Machine M.

1) In case a module looses its battery connection, a reverse power supply of this module via the CAN bus lines is prevented. For the PCA82C252 and the TJA1053 an external diode at the battery pin of the transceiver is required. This diode is required additionally to the control unit's polarity protection diode typically implemented at the battery connector of the entire module.

2. Upgrading a TJA1053 Design with the TJA1054

2.1. Overview

The TJA1054 is a fault-tolerant CAN transceiver suitable for networks including up to 32 nodes and is the compatible successor of the well-known TJA1053. Compared with the TJA1053, the TJA1054 provides several enhanced features:

- Extremely reduced electro-magnetic emission (EME)
- Very good electro-magnetic immunity (EMI)
- Enhanced bus failure management (short circuits to 5V are tolerated)
- Improved error signalling
- Improved behaviour during “Loss of Power” situations

The TJA1054 is designed to be downward compatible to the TJA1053 and can be used in most of the existing TJA1053 applications without any changes in hardware and software. Nevertheless, due to the enhanced functionality there are some points to be considered if the TJA1053 is replaced by the TJA1054.
The following chapters discuss all hardware and software issues in detail in order to allow a smooth migration from the TJA1053 to the TJA1054.
Special attention is paid to interoperability issues giving the confidence that both devices can be used simultaneously within one network. Validation showed that a “step-by-step” introduction of the TJA1054 into an existing TJA1053 system can be made without risk.

2.2. Hardware Issues

2.2.1. External Components

When the TJA1053 is replaced by a TJA1054, two external hardware components may be removed (see also figure 1) :

- Reverse current protection diode at pin BAT
- Pulse lengthening capacitor at pin ERR

The extra diode for the TJA1053 is needed to suppress a reverse power supply of the control unit if the battery connection of the entire unit was lost. For the TJA1053, a current flow from the CANL bus line backward to the pin BAT of the transceiver was possible if the transceiver was not powered. In some applications, this reverse current was high enough to supply the microcontroller unintentionally. The TJA1054 is internally protected against such reverse currents making the diode superfluous.

Reading the pin ERR during the normal CAN interrupt service routine was not possible for the TJA1053 in case of “open failures” on the bus lines. Here, the so-called “acknowledge bit” of any valid CAN message cleared an already detected “open failure” at the pin ERR. Therefore, an external lengthening capacitor was required for the TJA1053 in order to keep the detected failure signal valid until the interrupt service routine was executed by the host uC.
The TJA1054 does not require this extra lengthening capacitor since the pin ERR now internally keeps the failure signal active. (see also 11.2.1.)

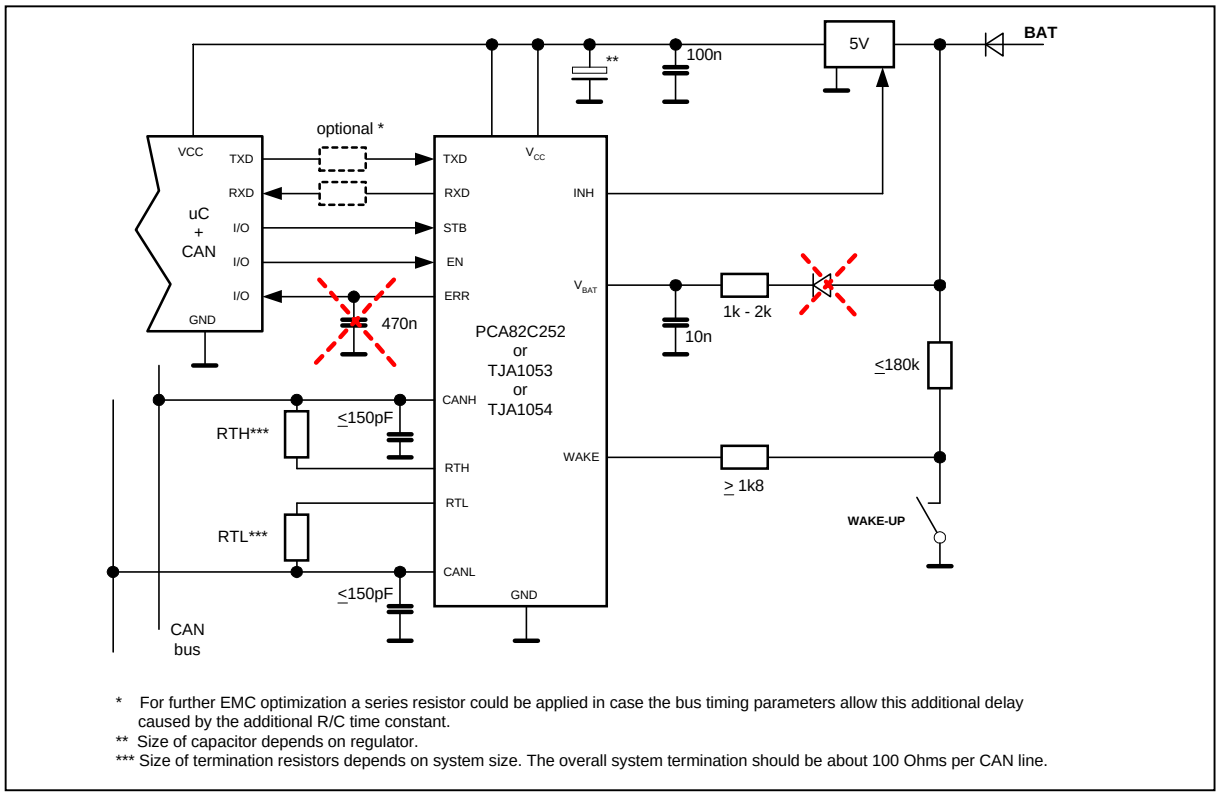


Figure 1 : Typical application circuitry using the TJA1053 and the TJA1054

2.2.2. Wake-up sensitivity at pin WAKE

The wake-up input of the TJA1054 is sensitive on both edges, whereas the TJA1053 was sensitive on the falling edge only. This has typically no impact on the application since such external wake-up events are usually pulses including both edges.
Another improvement of the TJA1054 is that wake-up events have higher priority than the goto-sleep command. Systems using the TJA1053 may lose such a wake-up event. Consequently, a TJA1053 node may keep sleeping without starting the voltage regulator although a wake-up request has been driven to the pin WAKE. The TJA1054 will now recognise any wake-up event independently from the current command setting of the host CPU.

2.2.3. Current consumption

The total current consumption of the TJA1054 is reduced compared to the TJA1053, especially during low-power modes. The slightly increased short circuit current of the CANH bus driver within the TJA1054 is compensated by its reduced normal mode supply current during dominant bus states. Thus, there is no impact to the applications power supply concept. But introduction of the TJA1054 provides a much lower sleep current per control unit now compared with the TJA1053.

Condition	TJA1053	TJA1054
Current consumption in Normal Mode, I_{CC}	6 mA recessive 29mA dominant	7 mA recessive 17mA dominant
Current consumption in Low-power Modes, $I_{BAT} + I_{CC}$	70uA	30uA

2.2.4. Operating Voltage Range

In order to increase the system performance during low battery conditions, the TJA1054 now allows operation down to 5V at the pin BAT, whereas the TJA1053 required at least 6V.

2.3. Software Issues

2.3.1. Error signalling via pin ERR

As already mentioned before, the behaviour of the error signalling at the pin ERR is improved within the TJA1054. This allows removing the external lengthening capacitor needed for the TJA1053 (see also 2.1). This new behaviour of the TJA1054 may have an impact on application software if the TJA1053 was used **without** external lengthening capacitor. Two scenarios are possible:

2.3.1.1. Software polls pin ERR

Application software polling the pin ERR will see fewer transitions if the TJA1053 is replaced by the TJA1054. Especially during “open failures” on the bus lines, the software load caused by ERR events is reduced if the TJA1054 is used.

2.3.1.2.Software reads pin ERR during CAN interrupt service only

Here, the “open failures” are now detected **and** signalled by the TJA1054 as desired, whereas the TJA1053 has signalled no problem. Thus, a simple migration to the TJA1054 automatically improves a software driven diagnosis function.

2.3.2. VCC Standby / PWON Standby

The VCC Standby Mode known from the TJA1053 is replaced by the so-called PWON Standby Mode in the TJA1054 (STB = 1; EN = 0). There is no change in functionality between both transceivers except for the CANL biasing level. The TJA1053 drives 5V to CANL through pin RTL and the termination resistor, while the TJA1054 now drives 12V to CANL using the same path. This has no impact on the overall system performance if both transceivers are mixed in one network. Software is not influenced since both transceivers provide the same status information to the microcontroller via ERR and RXD.

2.3.3. First Battery Connection, behaviour of pin INH

The TJA1053 allows to be set into Sleep Mode (INH floating) directly after first battery connection by driving the goto-sleep command to the control pins STB and EN (“01”). The TJA1054 needs to be set into Normal Mode before accepting the first goto-sleep command after first connection of the battery supply. After setting Normal Mode both devices behave identical concerning this item.
An internal power-on reset signal within the TJA1054 makes sure that the transceiver is reset successfully after power-up and the INH output is safely set to battery level. This internal reset signal is cleared whenever the Normal Mode is entered once. There are no special timing requirements to clear the internal reset signal thus software just has to set the Normal Mode via STB and EN followed by any other control code. Within most of the existing applications this is already implemented inside of the systems cold-start routines.

2.3.4. Goto-Sleep / Wake-up Priority

The pin INH of the TJA1053 does ignore wake-up events in case these wake-up events are present while the goto-sleep command is continuously driven to the transceiver via pins STB and EN (STB = 0 / EN = 1). After the goto-sleep filter time (see data sheets TJA1054/TJA1054A : “reaction time of goto sleep command”) the INH flip-flop is continuously cleared thus setting the pin INH to a floating condition. Wake-up events are forwarded to INH first with releasing the goto-sleep command. Thus a systems voltage regulator connected to INH will become disabled even if there is a pending wake-up request. Nevertheless RXD and ERR will signal the wake-up event with a LOW output level independently from the pending goto-sleep command.
For the TJA1054 this behaviour is improved and no wake-up event is lost with respect to the pin INH. Within the TJA1054 the wake-up events have a higher priority than the goto-sleep command. Thus any wake-up event will reset INH to a HIGH output level independently from the goto-sleep command. RXD and ERR will reflect the wake-up condition with a LOW output level as known from the TJA1053.
From software point of view it is highly recommended for both transceivers monitoring the pins RXD and/or ERR whenever the goto-sleep command was executed in order to detect a wake-up event

while the system should fall into sleep mode. INH might keep HIGH or become HIGH again caused by a wake-up event before the supply of the uC was successfully disabled. (see also 11.1.)

2.3.5. Other issues

Experiences with different software drivers have shown the advantage to implement a kind of CAN communication monitoring in software, expecting CAN bus events in certain time frames. At least a reception of messages or successful transmissions should appear in order to get confidence, that the CAN bus is still operating properly. This is especially important for recovery from dual bus failure situations towards single bus failure situations.
Due to the automatic transmit message repetition mechanism of a CAN protocol engine it might happen that a node retransmits a message forever in case there is no acknowledge received from the bus. This continuously transmitting node might lock the bus system and thus prevents other nodes to recover from a dual bus failure situation towards a single bus failure situation.
Therefore, whenever there is no response from the CAN bus within a reasonable time, pending transmission requests should be aborted in software. This will increase the system availability during certain bus failure conditions, which require single wire operation.

2.4. Interoperability : Mixed Systems with TJA1053 and TJA1054

2.4.1. Overview

During development of the TJA1054 special attention was paid to interoperability issues in order to allow a smooth migration of existing applications by simple replacement of the TJA1053. Particularly, the enhancements of the bus failure management (5V short circuits) have been included very carefully into the existing circuitry to avoid system hang-ups, if both transceivers are mixed in one system.
The TJA1054 is designed to replace the TJA1053 within running car series production without interoperability risk.
Interoperability of both devices has been proved in system simulation as well as in hardware investigation.
The key results of these investigations are :

- A pure TJA1054 network solves the known weaknesses of a TJA1053 system (wake-up of big networks with failure HxGND, short circuits to 5V ....)
- A mixed system of TJA1053 and TJA1054 has at least the same performance as the pure TJA1053 system; in some aspects the growing presence of TJA1054 nodes in the network even improves the overall system performance
- Taking into consideration the issues described in the previous chapters, mixed systems of both transceiver are possible at any ratio without restrictions

2.4.2. Hardware Interoperability Investigations

In order to investigate interoperability issues of the transceiver, a network with 25 nodes was set up and investigated in detail. A typical topology including star points was chosen according to real automotive applications. This topology includes cable stubs with more than 5 meters and more than 55 meters overall cable length.
Worst case scenarios were analysed including weak bus failure conditions, double failures, ground shifts and power supply drops. Especially, operating mode changes (Normal Mode / Standby / Sleep) were performed simultaneously with bus failure situations.

2.4.3. Results of Hardware Interoperability Investigation

The following table gives an overview about the mixed system investigations using the TJA1053 together with the TJA1054 in different mixing ratios. An assessment is made compared with a pure TJA1053 system with same topology.

Bus Failure		Standard Communication (incl. resistive failures)	Communication with Ground Shift (+/- 1.5V)	Communication at Low Battery Voltages	Mode Changes / Wake-up combined with Bus Failure Conditions	Communication with local Loss of Termination
0	**none**	✓	✓	✓	✓	✓
1	**H //**	✓	✓	✓	☺	☺
2	**L //**	✓	✓	✓	✓	✓
3	**HxBAT**	☺	✓	✓	✓	✓
3a	**HxVCC**	☺	☺	☺	☺	☺
4	**LxGND**	✓	☺	✓	✓	✓
5	**HxGND**	✓	✓	✓	☺	✓
6	**LxBAT**	✓	☺	✓	✓	✓
6a	**LxVCC**	✓	✓	✓	☺	✓
7	**HxL**	✓	✓	✓	✓	✓

Key :

(☺) mixed system behaves **better** than a pure TJA1053 system

(✓) mixed system behaves **equal** to a pure TJA1053 system

(👎) mixed system behaves **worse** than a pure TJA1053 system

2.5. Conclusion

Both transceivers, TJA1053 and TJA1054, are interoperable and can be used simultaneously within the same network. This allows migrating gradually from TJA1053 to TJA1054 in running car mass production.

Due to new features introduced with the TJA1054, existing TJA1053 applications need to be reviewed according to the comments within this report before replacing the transceiver.

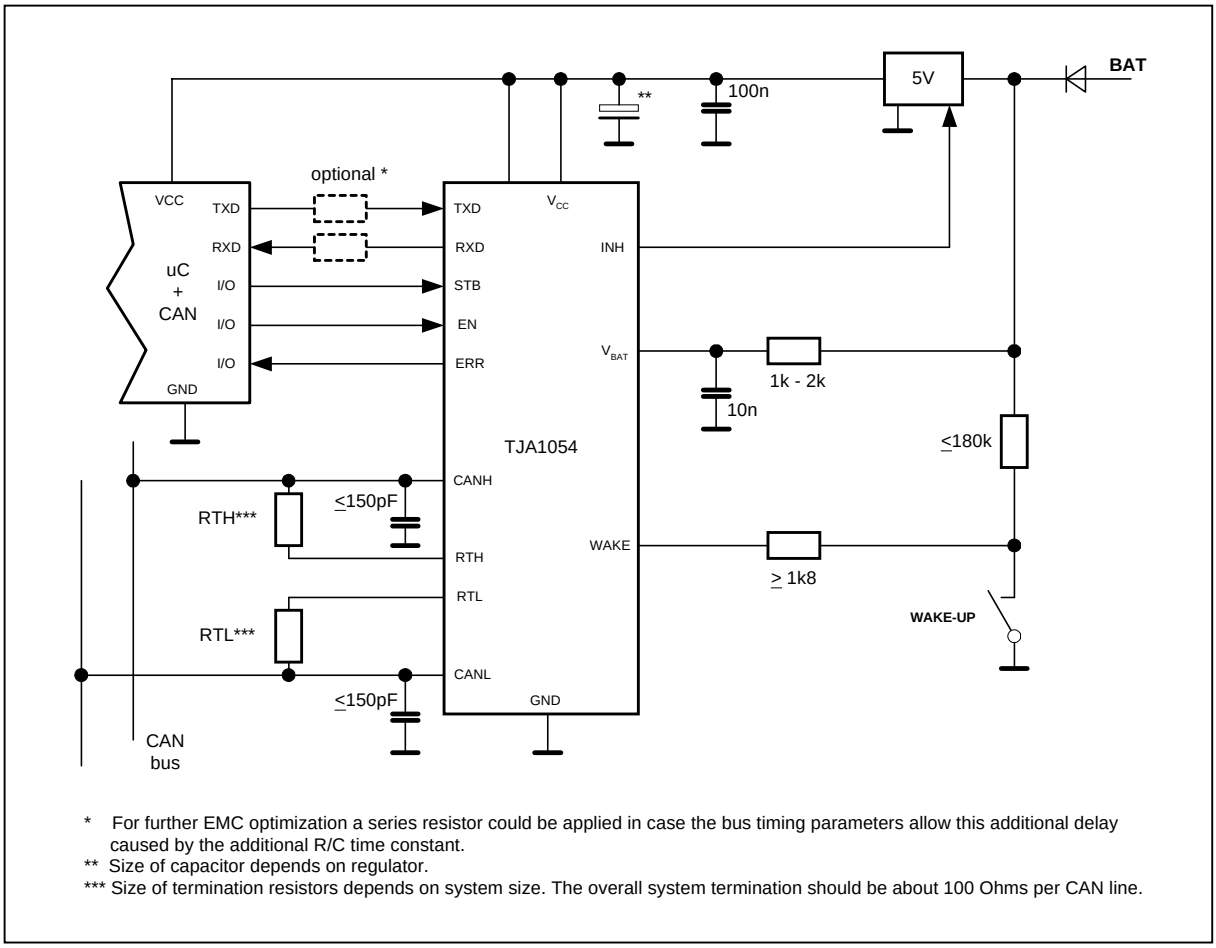
2.6. Migration Checklist

Item	TJA1053	TJA1054	Comment
Diode @ pin BAT	needed	can be removed	no reverse power supplying by TJA1054
Capacitor @ pin ERR	depends on software	can be removed	function is integrated into the TJA1054
Sensitivity of pin WAKE	falling edge only	both edges	check behaviour of system wake-up via pin WAKE
Goto-sleep command after first battery connection	always possible	possible only after Normal Mode was entered once	Internal power-on signal has to be cleared by setting the TJA1054 into Normal Mode after first battery connection
Goto-sleep command, priority of wake-up event	INH becomes floating the time goto-sleep is driven even if there is a wake-up coming	INH keeps HIGH if there is a wake-up coming during goto-sleep is driven	It is recommended to monitor pin RXD and/or pin ERR after goto-sleep in order to detect a wake-up event during the transition into Sleep Mode.

3. Mode Control with the TJA1054

3.1. Overview

The fault tolerant CAN transceiver TJA1054 provides an integrated functionality controlling an external voltage regulator in order to design low power CAN bus systems with remote and local wake-up capabilities. A dedicated INH pin allows disabling the entire power supply of a control unit, thus reducing the overall system power consumption to a minimum. The transceiver is the only supplied component during such a low-power state.
Following figure shows an application example using the TJA1054.



* For further EMC optimization a series resistor could be applied in case the bus timing parameters allow this additional delay caused by the additional R/C time constant.
** Size of capacitor depends on regulator.
*** Size of termination resistors depends on system size. The overall system termination should be about 100 Ohms per CAN line.

Figure 2 : Typical application of the TJA1054

As shown within Figure 2 the transceiver is powered directly from the battery supply via the pin BAT. This allows disabling the VCC supply entirely during time phases, the CAN bus is not required by the system. Therefore two control pins STB and EN coming from the host microcontroller are used to control the actual mode of operation like normal communication or low-power operation.
For wake-up purposes a battery-related WAKE pin is provided.
In addition to bus failure information and the CAN received bit stream, the pins ERR and RXD are used to signal wake-up requests towards the application controller.

3.2. Operating Modes

The two fail-safe coded pins STB and EN mainly control the power management of the TJA1054. They are defining directly the actual mode of operation as illustrated within Figure 3.
The following operating modes are implemented:

- Normal Mode — normal transceiver operation
- Goto Sleep — disables the external voltage regulator via INH after a certain time out
- Stby Sleep — similar to Goto Sleep, but INH is not affected
- PWON Stby — similar to Stby Sleep, but allows to read back the PWON flag indicating a power-on condition

All modes different from Normal Mode are low-power modes reducing the current consumption significantly.

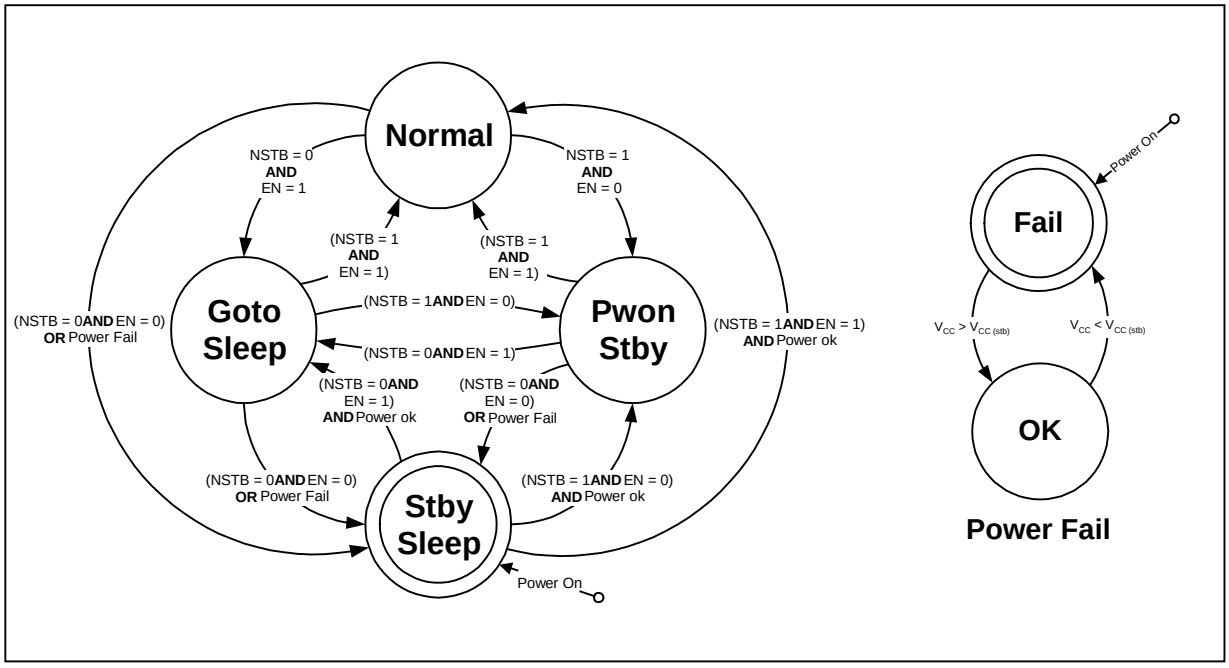


Figure 3 : Operating Modes of the TJA1054

Note, that a change from the power-on condition (STB and EN = “0”) is possible only, if the VCC supply is present. Whenever VCC falls below a certain level (see data sheet TJA1054: “supply voltage for forced Standby Mode”) the fail-safe Standby Mode is entered automatically (power-fail).
Depending on the selected mode of operation, the I/O pins provide different information for the application as described within the next chapters.

3.2.1. Normal Mode

During normal mode the transceiver is used to transmit data to the bus and to receive data from the CAN bus. Here the pin RXD reflects the bus signal and the pin ERR is used to signal bus failure conditions with an active LOW behaviour.

3.2.2. Goto Sleep

Entering Goto Sleep the transceiver immediately changes into low-power operation, while the pin INH is still kept active HIGH. Now an internal wake-up flip-flop is output via the pins RXD and ERR, if VCC is present. Thus both pin's signals can be used to wake-up the application with an active low signal. If the Goto Sleep state keeps present for a certain time (see data sheet TJA1054: "reaction time of goto-sleep command") the INH output of the TJA1054 becomes "floating" disabling the externally connected voltage regulator. The application can keep within the Goto Sleep state or switch over to Stby Sleep mode without any difference in behaviour of the transceiver.
Typically the application automatically changes towards Stby Sleep because the power supply of the host microcontroller becomes disabled during Goto Sleep and thus the control pins STB and EN are falling towards a LOW signal with the decreasing supply of the microcontroller.

3.2.3. Stby Sleep

If the system needs to keep the external voltage regulator active for some reason during low-power operation, this mode can be entered directly from normal mode. Then the pin INH keeps HIGH all time and the external voltage regulator stays alive. During this mode RXD and ERR are signalling a possible wake-up condition as described for the Goto Sleep state.
The internal "sub-modes" Standby and Sleep are distinguished only by the state of the pin INH. In case of a previous successful Goto Sleep procedure INH is floating during Stby Sleep.

3.2.4. PWON Stby

This mode behaves similar to Stby Sleep with the difference that the pin ERR allows reading back the internal PWON flag. This flag is set whenever the transceiver is powered with battery supply the first time. So the application can distinguish between a cold start situation caused by a system sleep or a cold start due to first battery connection of the device.

3.3. System Wake-up

Once the transceiver is not within Normal Mode there are the following possibilities to wake-up the system:

- Local wake-up using the local pin WAKE
- Remote wake-up caused by CAN bus traffic
- Mode change entering Normal Mode via STB and EN

3.3.1. Local wake-up

A local wake-up can be forced with an edge at the pin WAKE of the transceiver. A positive edge as well as a negative edge results in a system wake-up if the signal keeps constant for a certain time (see data sheet TJA1054: "required time on pin WAKE for local wake-up"). Thus short spikes are filtered and do not result in unwanted system wake-up conditions.
As a result of the edge at pin WAKE, the internal wake-up flip-flop is set and output at ERR and RXD. Additionally the pin INH becomes HIGH again, starting the external voltage regulator.
Note that the pin WAKE provides an internal weak pull-up current towards battery in order to provide a defined condition in case of open circuit.

3.3.2. Remote wake-up

Another possibility waking up the system is traffic on the CAN bus lines. Whenever the bus becomes dominant for a certain time within a CAN message (see data sheet TJA1054: "dominant time for remote wake-up on pin CANH or CANL") the internal wake-up flip-flop is set and the pin INH activates the external voltage regulator.

3.3.3. Mode change

The connected host microcontroller can directly switch the transceiver into Normal Mode by setting STB and EN High in case the VCC supply is present at the transceiver.

3.4. State diagrams

Within this chapter some state diagrams are collected showing the behaviour of the TJA1054 in more detail.

3.4.1. PWON Flag

The PWON flag is set whenever the transceiver is supplied the first time or the battery voltage drops below a certain limit (see data sheet TJA1054: “power-on flag voltage on pin BAT”). It is cleared when entering the Normal Mode.

3.4.2. Pin INH

The pin INH is controlled by the Goto Sleep state and the wake-up events. There is a priority of wake-up in order to make sure that any wake-up event keeps the external voltage regulator active independently of a goto-sleep command.
Note that a successful Goto Sleep is possible only if the Normal Mode was entered once after a power-on condition. The PWON flag has to be cleared making sure that the system was started successfully before entering the Sleep Mode the first time.

3.4.3. Wake-up Flag

An internal wake-up flag is set upon a local or remote wake-up event. This flag is cleared whenever the Normal Mode is entered via STB and EN. The content of this flag is signalled via RXD and ERR according to the corresponding state diagrams.

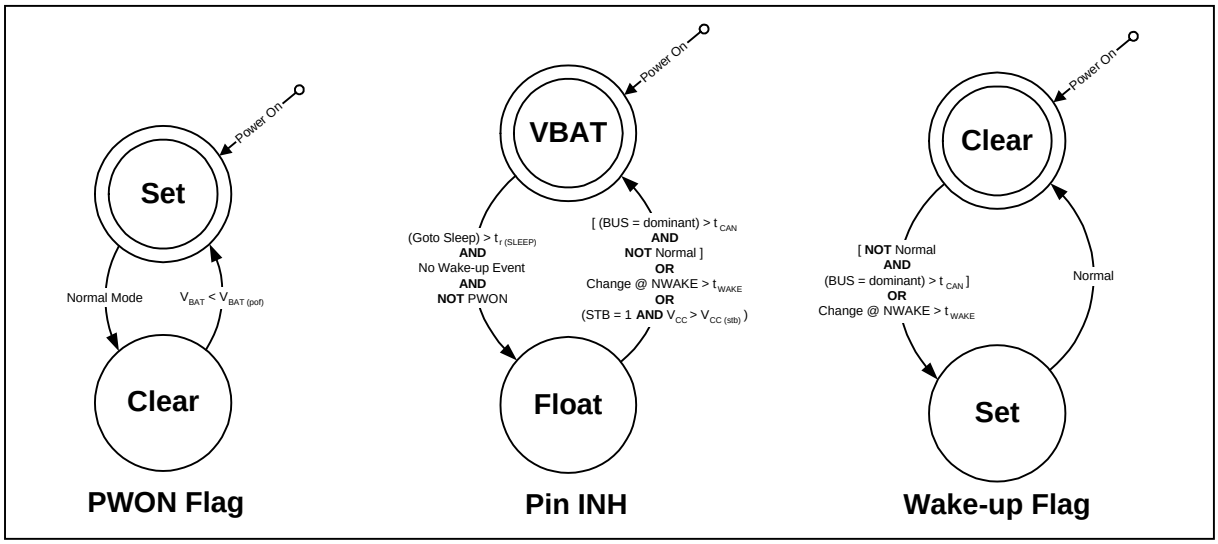


Figure 4 : State Diagrams, PWON Flag, pin INH and Wake-up Flag

3.4.4. Pin RXD

During Normal Mode the pin RXD reflects the actual bus signal. Immediately with changing into one of the low power modes, the content of the internal Wake-up Flag is reflected at pin RXD if the VCC supply of the transceiver is present. A wake-up condition is signalled active LOW.

3.4.5. Pin ERR

The pin ERR is used to signal bus failure conditions during normal operation with an active LOW behaviour. As soon as the transceiver is switched into Goto Sleep or Stby Sleep Mode the internal Wake-up Flag is reflected via ERR similar to the pin RXD. A change towards PWON Stby immediately switches ERR to the internal PWON Flag. A power-on condition is signalled active LOW. Please take care that the external loading to the pin ERR may cause a delay changing the level from LOW to HIGH. Typically a uC-port pin causes a load of some 10pF to the pin ERR. Due to the relatively weak pull-up behaviour of the pin ERR, charging this wire may need relevant time for fast operating software (see also 11.3.).

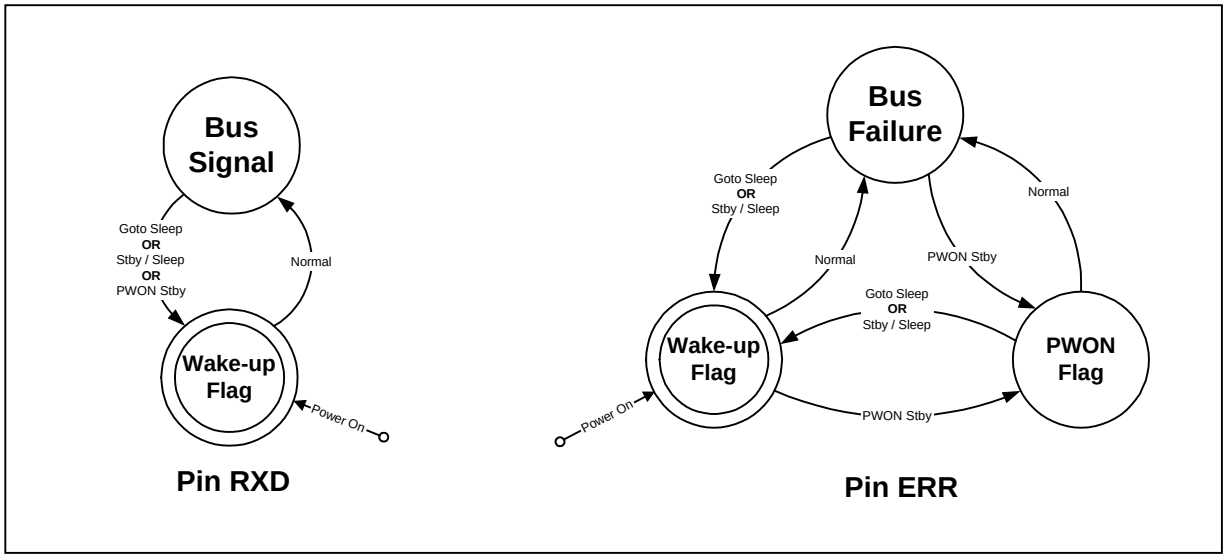


Figure 5 : State Diagrams, pins RXD and ERR

4. Vcc Supply and Recommended Bypass Capacitance

4.1. List of used Abbreviations

Table 4-1 : Used abbreviations

Symbol	Description
I_{cc_dom}	Supply current at pin VCC while driving a dominant bit **with** a certain load to the pins
I_{cc0_dom}	Supply current at pin VCC while driving a dominant bit **without** any load to the pins
I_{CANH_dom}	Output current of pin CANH while driving a dominant bit with nominal bus load of 100 Ohms in total
I_{RTL_dom}	Output current of pin RTL while driving a dominant bit with a certain load
I_{cc_rec}	Supply current at pin VCC while driving a recessive bit
$I_{cc\_norm\_avg}$	Average supply current at pin VCC assuming no bus failure and continuous sending
$I_{cc\_sc1\_dom}$	Supply current at pin VCC driving a dominant bit while CANH is shorted to GND
$I_{CANH\_sc1\_dom}$	Output current of pin CANH driving a dominant bit while CANH is shorted to GND
$I_{cc\_sc1\_avg}$	Average supply current at pin VCC assuming CANH shorted to GND and continuous sending
ΔI_{cc_sc1}	Supply current change at pin VCC in case a dominant bit is driven while CANH is shorted to GND
$I_{cc\_sc2\_dom}$	Supply current at pin VCC driving a dominant bit while CANH **and** CANL are shorted to GND
$I_{RTL\_sc\_dom}$	Output current of pin RTL while driving a dominant bit with CANL shorted to GND
ΔI_{cc_sc2}	Supply current change at pin VCC in case a dominant bit is driven while CANH and CANL are shorted to GND
V_{CC}	Supply voltage at pin VCC
V_{CANL_dom}	Voltage level on CANL while a dominant bit is driven
R_T	Termination resistor connected to pins RTL and RTH
t_{dom_max}	Maximum possible continuous dominant drive time
ΔV_{max}	Maximum allowed voltage change at pin VCC
C_{BUFF}	Required buffer capacitance in case the voltage regulator does not deliver extra current within t_{dom_max}

4.2. Summary

In order to properly dimension the Vcc supply of the fault-tolerant CAN transceivers two parameters have to be taken into account:

1) the average supply current
2) the peak supply current

The average supply current is needed to calculate the thermal load of the required Vcc voltage regulator. The peak supply current may flow in case of certain bus failure conditions for a certain time and thus has an impact on the power supply buffering.

The Vcc supply of the transceiver is recommended to support the characteristics as follows:

Table 4-2 : Overview of supply currents

Item	PCA82C252	TJA1053	TJA1054
Average Vcc supply current without bus failures	44.5 mA	44.5 mA	41 mA
Average Vcc supply current at presence of single bus failures	74.5 mA	74.5 mA	76 mA
Worst case peak Vcc supply current at presence of single bus failure (for 6 bit times max.)	139 mA	139 mA	141 mA
Worst case peak Vcc supply current at presence of dual bus failures (for 17 bit times max.)	140 mA	140 mA	142 mA

The capacitive buffering needed for the transceiver depends on the systems power concept and the regulator characteristic of the used voltage regulator chip.

In case the transceiver has a **separated** Vcc power supply apart from the microcontroller, the peak supply current during single bus failures is relevant because here the communication medium has to keep unaffected. The worst case dual failure situation is not relevant since here the communication medium is completely out of operation and the transceiver does not need to be supplied anymore. Such systems are recommended to provide a bypass capacitance of **47 uF** in order to support single wiring faults. **Depending on the regulator behaviour this capacitance may become smaller if the regulation time constant is fast enough.**

In case the transceiver's Vcc power supply is **shared** with its host microcontroller, the peak supply current during the worst case dual failure situation has to be taken into account. This is because the uC has to keep a proper supply even if there is no CAN communication possible at all. Such systems are recommended to provide a bypass capacitance of **150uF**. **Depending on the regulator behaviour this capacitance may become much smaller if the regulation time constant is fast enough.**

This capacitance can be implemented as a separate component or alternatively through a corresponding increase of the capacitance of the bypass capacitor being located at the Vcc voltage regulator.

In the following, relevant cases are considered in more detail.

4.3. Average Supply Current at Absence of Bus Short-Circuit Conditions

In recessive state the different transceivers are consuming a Vcc supply current as listed in the corresponding data sheets. In dominant state the Vcc supply current is calculated by the addition of the IC-internal supply current (see data sheet TJA1054: “no load” condition) and the output current at pins CANH and RTL.

4.3.1. Maximum dominant supply current (without bus wiring faults)

$$I_{cc\_dom} = I_{cc0\_dom} + I_{CANH\_dom} + I_{RTL\_dom} \quad (1)$$

$$I_{RTL\_dom} = (Vcc - V_{CANL\_dom}) / R_T \quad (2)$$

4.3.1.1.Example calculation

Maximum dominant supply current without bus wiring faults:

Item from Data Sheet / Assumptions	*Symbol*	*PCA82C252*	*TJA1053*	*TJA1054*
Max. Vcc supply current dominant, no load	I_{cc0_dom}	35 mA	35 mA	27 mA
CANH dominant current	I_{CANH_dom}	40 mA	40 mA	40 mA
Assumed termination resistor	R_T	1 k	1 k	1 k
Assumed CANL dominant voltage	V_{CANL_dom}	1 V	1 V	1 V

PCA82C252 : $I_{cc\_dom\ 252}$ = 35mA + 40 mA + (5V - 1V) / 1k = 79 mA max. (Ex 1.1)

TJA1053 : $I_{cc\_dom\ 1053}$ = 35mA + 40 mA + (5V - 1V) / 1k = 79 mA max. (Ex 1.2)

TJA1054 : $I_{cc\_dom\ 1054}$ = 27mA + 40 mA + (5V - 1V) / 1k = 71 mA max. (Ex 1.3)

4.3.2. Thermal considerations (without bus wiring faults)

For thermal considerations the average supply current at pin Vcc is relevant considering the transmit duty cycle. In the following example a continuously transmitting node is assumed. This might happen e.g. if a node starts a transmission while the rest of the network does not respond with an acknowledge for some reason. Typically a much lower duty cycle is relevant since a node transmits messages within certain time slots only, depending on the applications network management. With an assumed transmit duty cycle of 50% on pin TxD, the maximum average supply current is

$$I_{cc\_norm\_avg} = 0.5 * (I_{cc\_rec} + I_{cc\_dom}) \quad (3)$$

4.3.2.1.Example calculation

Thermal considerations without bus wiring faults:

Item	*Symbol*	*PCA82C252*	*TJA1053*	*TJA1054*
Vcc supply current recessive, max.	I_{cc_rec}	10 mA	10 mA	11 mA

PCA82C252 : $I_{cc\_norm\_avg\ 252}$ = 0.5 * (10mA + 79mA) = **44.5 mA max.** (Ex 3.1)

TJA1053 : $I_{cc\_norm\_avg\ 1053}$ = 0.5 * (10mA + 79mA) = **44.5 mA max.** (Ex 3.2)

TJA1054 : $I_{cc\_norm\_avg\ 1054}$ = 0.5 * (11mA + 71mA) = **41 mA max**. (Ex 3.3)

4.4. Average Supply Current at Presence of a Short-Circuit of one Bus Wire

The maximum Vcc supply current occurs with a bus wire short-circuit between CANH and GND. In this case the CANH outputs a maximum short circuit current in dominant state (see data sheets). For thermal considerations the average supply current is relevant. For buffering considerations the maximum dominant supply current is relevant.

4.4.1. Maximum dominant supply current (with CANH shorted to GND)

$$I_{cc\_sc1\_dom} = I_{cc0\_dom} + I_{CANH\_sc1\_dom} + I_{RTL\_dom} \quad (t \leq 6 \text{ bit times}) \qquad (4)$$

The 6-bit time limitation is caused by a supposed Error Flag to be sent by the CAN Controller.

4.4.1.1.Example calculation

Maximum dominant supply current with CANH shorted to GND:

Item	Symbol	PCA82C252	TJA1053	TJA1054
CANH dominant current, short circuit	$I_{CANH\_sc1\_dom}$	100 mA	100 mA	110 mA

PCA82C252 : $I_{cc\_sc1\_dom\ 252}$ = 35mA + 100 mA + (5V - 1V) / 1k = **139 mA max.** (Ex 4.1)

TJA1053 : $I_{cc\_sc1\_dom\ 1053}$ = 35mA + 100 mA + (5V - 1V) / 1k = **139 mA max.** (Ex 4.2)

TJA1054 : $I_{cc\_sc1\_dom\ 1054}$ = 27mA + 110 mA + (5V - 1V) / 1k = **141 mA max.** (Ex 4.3)

4.4.2. Thermal considerations (with CANH shorted to GND)

For thermal considerations the average supply current at pin Vcc is relevant considering the transmit duty cycle. With a transmit duty cycle of 50% on pin TxD, the maximum average supply current at CANH to GND short-circuit is:

$$I_{cc\_sc1\_avg} = 0.5 * (I_{cc\_rec} + I_{cc\_sc1\_dom}) \qquad (5)$$

4.4.2.1.Example calculation

Thermal considerations with CANH shorted to GND:

PCA82C252 : $I_{cc\_sc1\_avg\ 252}$ = 0.5 * (10mA + 139mA) = **74.5 mA max.** (Ex 5.1)

TJA1053 : $I_{cc\_sc1\_avg\ 1053}$ = 0.5 * (10mA + 139mA) = **74.5 mA max.** (Ex 5.2)

TJA1054 : $I_{cc\_sc1\_avg\ 1054}$ = 0.5 * (11mA + 141mA) = **76 mA max.** (Ex 5.3)

4.4.3. Vcc extra supply current in single fault condition

Compared to the quiescent current in recessive state the maximum **extra** supply current when the CANH driver is turned on with CANH shorted to GND is needed to calculate the required worst case Vcc buffer capacitance. This extra supply current has to be buffered for up to 6 bit times, depending on the applications voltage regulator.

$$\Delta I_{cc\_sc1} = I_{cc\_sc1\_dom} - I_{cc\_rec} \quad \textbf{(6)}$$

4.4.3.1.Example calculation

Vcc extra supply current in case of single fault condition.

Item	*Symbol*	*PCA82C252*	*TJA1053*	*TJA1054*
Min Vcc supply current, recessive	I_{cc_rec}	3,5 mA [1)]	3,5 mA [1)]	4 mA

1) The minimum quiescent current is estimated since this value is not specified for the PCA82C252 and the TJA1053.

PCA82C252 : $\Delta I_{cc\_sc1\ 252}$ = 139 mA - 3.5 mA = **135.5 mA max.** (Ex 6.1)

TJA1053 : $\Delta I_{cc\_sc1\ 1053}$ = 139 mA - 3.5 mA = **135.5 mA max.** (Ex 6.2)

TJA1054 : $\Delta I_{cc\_sc1\ 1054}$ = 141 mA - 4 mA = **137 mA max.** (Ex 6.3)

4.5. Worst Case Max Vcc Supply at Presence of a Dual Short Circuit

The worst case max. Vcc supply current is flowing in case of a **dual short-circuit** of the bus lines CAN_H and CAN_L to ground. In this case no communication is possible. Nevertheless the application supply should be able to deliver a proper Vcc for the microcontroller in order to prevent faulty operation.
If there is a **separate** voltage regulator available supplying the transceiver exclusively, **no care** has to be taken on this dual short circuit condition since the transceivers are behaving fail safe in case of under voltage conditions and the uC is still powered properly by its own supply.

In case of a **shared** voltage supply of transceiver and microcontroller this dual fault condition is relevant to dimension the required buffer capacitor.

4.5.1. Max Vcc supply current in worst case dual fault condition

$$\mathbf{I_{cc\_sc2\_dom} = I_{cc0\_dom} + I_{CANH\_sc1\_dom} + I_{RTL\_sc\_dom}} \qquad \mathbf{(t \leq 17 \text{ bit times })} \qquad \mathbf{(7)}$$

$$\mathbf{I_{RTL\_sc\_dom} = Vcc / R_T} \qquad \mathbf{(8)}$$

The 17-bit time limitation is caused by the CAN protocol. Due to the dual fault condition with CANH and CANL shorted to GND the pin RxD of the transceiver is continuously clamped recessive (CANL to GND forces CANH operation; CANH is clamped recessive).

The moment the CAN controller starts a transmission, this dominant Start Of Frame bit is not fed back via RxD and thus forces an error flag due to the bit failure condition (TX Error Counter incremented by 8). This first bit of the error flag again is not reflected at RxD and forces the next error flag (TX Error Counter + 8).

Latest after 17 bit times, depending on the TX Error Counter Level before starting this transmission, the CAN controller reaches the Error Passive limit (128) and stops sending dominant bits. Now a sequence of 25 recessive bits follows (8 Bit Error Delimiter + 3 Bit Intermission + 8 Bit Suspend Transmission) and the Vcc current becomes reduced to the recessive one.
From now on only single dominant bits (Start Of Frame) followed by 25 recessive bits (Passive Error Flag + Intermission + Suspend Transmission) are output until the CAN controller enters the Bus Off State.

So, for dimensioning the Vcc voltage source in this worst case dual failure scenario, up to 17 bit times might have to be buffered by a bypass capacitor depending on the regulation capabilities of the used voltage supply.

4.5.1.1.Example calculation

Max Vcc supply current in worst case dual fault condition:

PCA82C252 :	$I_{cc\_sc2\_dom\ 252}$ = 35 mA + 100 mA + 5V / 1k = **140 mA max.**	(Ex 7.1)
TJA1053 :	$I_{cc\_sc2\_dom\ 1053}$ = 35 mA + 100 mA + 5V / 1k = **140 mA max.**	(Ex 7.2)
TJA1054 :	$I_{cc\_sc2\_dom\ 1054}$ = 27 mA + 110 mA + 5V / 1k = **142 mA max.**	(Ex 7.3)

4.5.2. Vcc extra supply current in dual fault condition

Compared to the quiescent current in recessive state the maximum **extra** supply current when the CANH driver is turned on in dual short-circuit condition is needed to calculate the required worst case Vcc buffer capacitance. This extra supply current has to be buffered for that time the applications voltage regulator needs to react.

$$\Delta I_{cc\_sc2} = I_{cc\_sc2\_dom} - I_{cc\_rec} \quad \textbf{(9)}$$

4.5.2.1.Example calculation

Vcc extra supply current in case of dual fault condition.

Item	*Symbol*	*PCA82C252*	*TJA1053*	*TJA1054*
Min Vcc supply current, recessive	I_{cc_rec}	3,5 mA [1)]	3,5 mA [1)]	4 mA

1) The minimum quiescent current is estimated since this value is not specified for the PCA82C252 and the TJA1053.

PCA82C252 : $\Delta I_{cc\_sc2\ 252}$ = 140 mA - 3.5 mA = **136.5 mA max.** (Ex 9.1)

TJA1053 : $\Delta I_{cc\_sc2\ 1053}$ = 140 mA - 3.5 mA = **136.5 mA max.** (Ex 9.2)

TJA1054 : $\Delta I_{cc\_sc2\ 1054}$ = 142 mA - 4 mA = **138 mA max.** (Ex 9.3)

4.6. Calculation of worst-case bypass capacitor

Depending on the power supply concept, the required worst-case bypass capacitor can be calculated. In case of a **separate Vcc** supply for the transceiver only, the extra supply current ΔI_{cc_sc} in case of the **single fault condition** has to be taken with a maximum of 6 dominant bit times.

If the transceiver and the host microcontroller are supplied from the same regulator (**shared Vcc supply**), the extra supply current ΔI_{cc_sc} in case of the **dual fault condition** has to be taken with a maximum of 17 dominant bit times.

$$C_{BUFF} = \Delta I_{cc\_sc} * t_{dom\_max} / \Delta V_{max} \quad \textbf{(10)}$$

The capacitor C_{BUFF} is needed if the voltage regulator is **not** able to deliver any extra current within the maximum dominant output drive t_{dom_max} during the dual fault condition.

4.6.1. Example calculation, separate supplied transceiver @ 83,33kBit/s

In case of a separate transceiver supply the bypass capacitance has to be calculated based on the single fault condition with CANH shorted to GND. Here the dual fault is not relevant.

Assumption of 83,33 kBit/s : t_{dom_max} = 6 * 12 us = 72 us
Maximum allowed Vcc voltage drop : ΔV_{max} = 0.25V

PCA82C252 : $C_{BUFF\ 252}$ = 135.5 mA * 72 us / 0.25 V = **39 uF** (Ex 10.1)

TJA1053 : $C_{BUFF\ 1053}$ = 135.5 mA * 72 us / 0.25 V = **39 uF** (Ex 10.2)

TJA1054 : $C_{BUFF\ 1054}$ = 137 mA * 72 us / 0.25 V = **39,5 uF** (Ex 10.3)

In this example the bypass capacitance to be reserved for the Vcc supply of the transceiver is recommended to be 39,5 uF minimum at 83,33 kBit/s. It may become smaller, if the used voltage regulator is able to deliver an extra current within t_{dom_max}.

4.6.2. Example calculation, shared supply

In case of a shared supply concept the bypass capacitance has to be calculated based on the worst case dual fault condition in order to keep the uC supply stabile:

Assumption of 83,33 kBit/s : t_{dom_max} = 17 * 12 us = 204 us
Maximum allowed Vcc voltage drop : ΔV_{max} = 0.25V

PCA82C252 : $C_{BUFF\ 252}$ = 136.5 mA * 204 us / 0.25 V = **111.4 uF** (Ex 10.1)

TJA1053 : $C_{BUFF\ 1053}$ = 136.5 mA * 204 us / 0.25 V = **111.4 uF** (Ex 10.2)

TJA1054 : $C_{BUFF\ 1054}$ = 138 mA * 204 us / 0.25 V = **113 uF** (Ex 10.3)

In this example the bypass capacitance to be reserved for the Vcc supply of the transceiver is recommended to be 113 uF minimum at 83,33 kBit/s. It may become smaller, if the used voltage regulator is able to deliver an extra current within t_{dom_max}.

5. Bus Termination and EMC issues

5.1. How to dimension the Bus Termination Resistor values, some basic rules

The fault tolerant transceivers are designed to deliver optimum system behaviour at a total termination resistance of 100 Ohms. This means that the CANH line is terminated with 100 Ohms as well as the CANL line. Because the termination of this fault tolerant system is distributed all over the network, each of the transceivers has to deliver only a part of the total 100 Ohm termination. So depending on the overall system size the single nodes local termination resistors have to be calculated.

Termination resistors are connected within each control unit to the corresponding pins RTH and RTL of the transceivers.

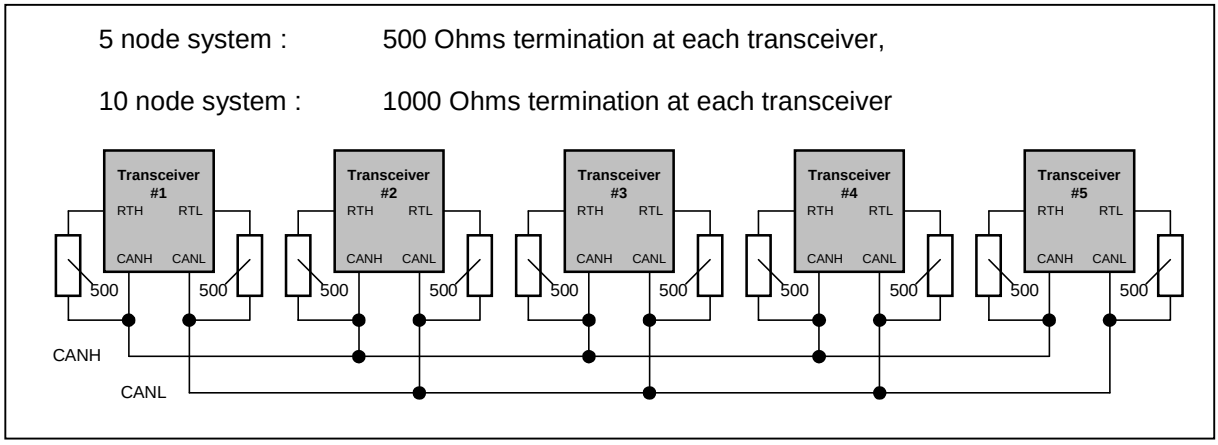


Figure 6 : Example Network with 5 nodes, 500 Ohms termination at each node

It is not required that each transceiver in the system has the same termination resistor value. In total the termination should result in 100 Ohms. It is not recommended to terminate the entire system lower than 100 Ohms since the CAN output drivers are limited to a load of 100 Ohms.

The minimum termination resistor value allowed per transceiver is 500 Ohms due to the driving capability of the pins RTL and RTH. So within systems with less than 5 transceivers it is not possible to achieve the 100 Ohm termination optimum. In practice this is typically no problem because such “small” systems will have less bus cable lengths compared to bigger networks and thus have no problem with a higher total termination resistances.

It is recommended not to exceed approximately 6kOhms termination at a single transceiver in order to provide a good EMI (Electro Magnetic Immunity) performance of the system in case of interrupted bus wires. Nevertheless up to 16kOhms are specified for the transceivers.

5.1.1. Variable System Size, Optional Nodes

In case of variable system sizes with optional nodes it is recommended to achieve a total termination resistance close to 100 Ohms provided by the standard nodes which are always present. The optional nodes should have the higher termination resistances then. Due to EMI issues it is recommended not to exceed approx. 6kOhms for the optional nodes.

5.1.1.1.Example calculation, Variable System Size

The entire example system has 15 nodes in total, 5 nodes of this system are optional ones and only implemented if required:

Termination of the 10 standard nodes :	1.2 kOhm per node
Termination of the 5 optional nodes :	3 kOhm per node
Total system termination, standard nodes only :	1.2 kOhm / 10 nodes =
	120 Ohms (...close to 100)
Total system termination, 15 nodes :	(3 kOhm / 5 nodes) parallel to 120 Ohms =
	100 Ohms

There is no general rule how to distribute the termination within the network. A rule of thumb is :

“The longer the cable stub, the lower the local termination.”

5.2. Tolerances of Bus Termination Resistors, EMC Considerations

The symmetry of the termination resistors within a single node has a major impact to the systems EME (Electro Magnetic Emission) behaviour. Thus it is important to have well matched termination resistors within each control unit. This means that the RTH resistor should have exactly the same value compared to the RTL resistor within one control unit in order to get the same time constant on each bus wire during signal transitions. Two different control units might have completely different termination values. (see also 5.1.1. “Variable system size, optional nodes”).
The principle to achieve a good EME performance is that the differential signal on the bus wires eliminates any emission due to compensation effects if both CAN wires are carrying exactly the same signal, but with inverse polarities.
Here the transceiver can only provide a perfect symmetry for the dominant transitions by design. The recessive transitions are mainly driven by the termination resistors and the network cables itself. So not only the transceiver’s output drivers have an impact to the EME performance but also the termination and the cable symmetry.

It is recommended to provide a termination resistor accuracy (RTH compared to RTL) within the same node of 1% or lower. Also the bus cable has to be at least a twisted pair cable in order to achieve a symmetrical capacitive load for both bus wires resulting in a good EMC performance.

It is obvious that also the layout of printed circuit boards has a significant impact to the EMC behaviour if the CAN lines have different capacitive loads due to different wire lengths.

5.3. Output Current and Power Dissipation of Bus Termination Resistors R_T

5.3.1. Summary

The bus termination resistors R_T being connected to the fault tolerant transceivers are recommended to withstand the following power dissipations (@ $R_T \geq 1000$ Ohms):

PCA82C252 : 64 mW
TJA1053 : 64 mW
TJA1054 : 31,7 mW

The following chapters are discussing this issue in more detail.

5.3.2. Average power dissipation, no bus failures

In order to dimension the power dissipation of the termination resistors connected to pins RTH and RTL, the average power dissipation between dominant and recessive bits has to be taken into account. Additionally a worst case ground offset of the certain module has an impact.
CAN frames are assumed to have a ratio of dominant bits in the range of 0.75 worst case because of stuffing and fixed recessive frame segments. Thus the average power dissipation is calculated as follows:

$$\mathbf{P_{avg} = 0.75 * (V_{cc} + V_{GND})^2 / R_T} \qquad \mathbf{(11)}$$

5.3.2.1.Example calculation, average power dissipation

Assumption : R_T = 1000 Ohms

$P_{avg} = 0.75 * (5V + 1{,}5V)^2 / 1000\ \text{Ohms} =$ **31.7 mW** (Ex 11.1)

5.3.3. Maximum continuous power dissipation (single bus failure)

Because the PCA82C252 and the TJA1053 do not provide a failure detector for CANH short circuits to Vcc the maximum continuous current flows in case CANH has a short circuit to 8V. This is the maximum detection threshold for CANH to battery short circuit conditions.

For the TJA1054 this threshold is 1.85V since shorts to Vcc are detected by this transceiver.

$$\mathbf{P_{cont} = (V_{det\ max})^2 / R_T} \qquad \mathbf{(12)}$$

5.3.3.1.Example calculation, maximum continuous power dissipation

Assumption : R_T = 1000 Ohms, connected to RTH

PCA82C252 : $P_{cont} = (8\ V)^2 / 1000\ \text{Ohms} =$ **64 mW** (Ex 12.1)
TJA1053 : $P_{cont} = (8\ V)^2 / 1000\ \text{Ohms} =$ **64 mW** (Ex 12.2)
TJA1054 : $P_{cont} = (1.85\ V)^2 / 1000\ \text{Ohms} =$ **3.4 mW** (Ex 12.3)

5.3.4. Maximum peak power dissipation (single bus failure)

A peak current will flow in case of short circuits of CANH to VBAT. After the device specific detection time, the bus failure detector will switch off the bias on RTH. Thus this peak current does only flow for a short time.

$$P_{peak} = V_{BAT}^2 / R_T \qquad (t < t_{det\_HBAT}) \qquad (13)$$

5.3.4.1.Example calculation, maximum peak power dissipation

Item	*Symbol*	*PCA82C252*	*TJA1053*	*TJA1054*
Maximum Failure Detection Time, CANH shorted to VBAT	t_{det_HBAT}	60 us	60 us	8 ms

Assumptions : R_T = 1000 Ohms, V_{BAT} = 27V

PCA82C252 : P_{peak} = (27 V) ^{2} / 1000 Ohms = **730 mW** for less than **60 us** (Ex 13.1)

TJA1053 : P_{peak} = (27 V) ^{2} / 1000 Ohms = **730 mW** for less than **60 us** (Ex 13.2)

TJA1054 : P_{peak} = (27 V) ^{2} / 1000 Ohms = **730 mW** for less than **8 ms** (Ex 13.3)

Because this peak current does flow for a very short time only, it typically has no relevance for dimensioning the termination resistors. Most important is the average power dissipation for the TJA1054 (23,7 mW) and the maximum continuous power dissipation for the TJA1053 / PCA82C252 (64 mW) since these are the worst case conditions for the corresponding devices.

6. ESD Protection

The fault-tolerant transceiver PCA82C252, TJA1053 and TJA1054 are providing an integrated ESD protection circuitry. According to the data sheets of these products, up to 2kV human body model as well as 200V machine model are allowed. These limits are defined for the stand-alone product, which is not mounted within a real application. The ESD limits will get further improved, if the transceivers are mounted on a printed circuit board due to the additional capacitive loading by wires and connectors.

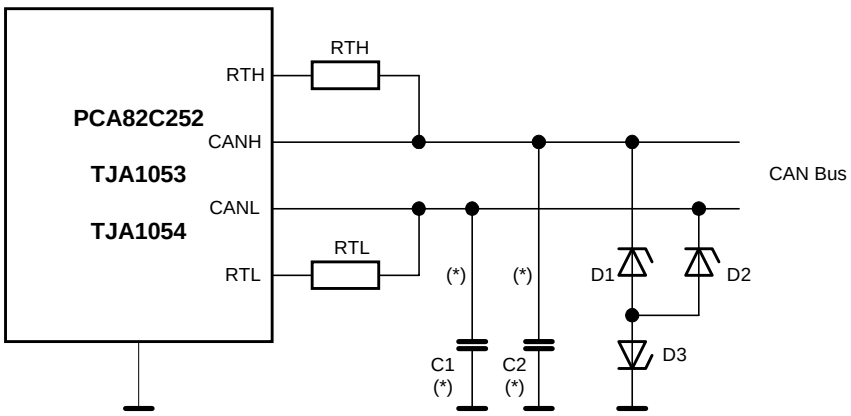
6.1. Improved ESD capability of TJA1054A

Since there is a demand on further ESD improvements integrated within the transceiver, the TJA1054 has become improved in terms of ESD with its successor product TJA1054**A**. The TJA1054A allows up to 4kV human body and 300V machine model without external components. The TJA1054A is fully compatible and interoperable to the previous transceivers.

ESD Item		PCA82C252 / TJA1053 / TJA1054	TJA1054**A**
Human Body Model	pins RTH, RTL, CANH, CANL	2kV	**4kV**
	other pins	2kV	2kV
Machine Model	all pins	200V	**300V**

6.2. Optional external ESD Improvement

In case the ESD requirements of certain applications could not be reached with the transceiver directly, external clamping diodes or varistors could be optionally connected to the application's CAN bus interface.
The purpose of the below presented circuit approach is to limit the peak voltages being present at the IC pins CANH and CANL of the fault-tolerant CAN transceiver when a CAN bus line is being subjected to ESD pulses.



D1 = D2 = D3 : stand-off voltage > max. bus line DC voltage, e.g. BZG04-27 or equiv. for bus line voltages ≤ +27V
C1 = C2 = 100 pF to 330 pF
(*) Note: minimize inductance & length of C1 and C2 leads

Figure 7 : Optional ESD Protection, Example

7. Series Resistor at Pin BAT

The following considerations are recommended for the determination of the series resistor (R_{BAT}) being attached to the supply input BAT (pin 14) of the TJA1053 / TJA1054 transceiver products.
The minimum recommended series resistance is about 1 kOhm for protection against automotive transients. On the other hand the series resistance implies voltage drop on the battery supply and therefore lowers the minimum operating voltage. The voltage drop across the R_{BAT} series resistance can be calculated with the following consideration:

Sym.	Parameter	PCA82C252	TJA1053	TJA1054
V_{BAT}	Minimum operating voltage	6V	6V	5V
I_{BAT}	Basic BAT supply current (V_{BAT} = 12V)	75 uA	90 uA	50 uA (12V) 125 uA (5 to 27V)
I_{IL}	WAKE input current	250 uA	70 uA	10 uA
I_{INH}	Max INH load (when used)	180 uA	180 uA	180 uA
R_{RTL}	RTL to V_{BAT} switch series resistance in low power modes	R_{RTL} = 10k to 28k	R_{RTL} = 8k to 23k	-
I_{RTL}	RTL current in low power modes	-	-	I_{RTL} = 0.3mA to 1.25mA
R_T	Bus termination resistance being attached to pin RTL	0.5k to 16k	0.5k to 16k	0.5k to 16k
I_{BATN}	Total BAT current in **normal mode**	75 uA + 250 uA + 180 uA = 505 uA	90 uA + 70 uA + 180 uA = 340 uA	125 uA + 10 uA + 180 uA = 315 uA
	Max R_{BAT} voltage drop with R_{BAT} = 1k in normal mode	0.51V	0.34V	0.32V
I_{RTL}	Max RTL load (applies only to low-power modes)	$V_{BAT}/(R_{RTL} + R_T)$ = 12V/(8k + 0.5k) = 1.41 mA	$V_{BAT}/(R_{RTL} + R_T)$ = 12V/(8k + 0.5k) = 1.41 mA	1.25 mA
I_{BATL}	Total BAT current in **low-power mode** (V_{BAT} = 12V)	0.51 mA + 1.41 mA = 1.92 mA	0.34 mA + 1.41 mA = 1.75 mA	0.32 mA + 1.25 mA = 1.57 mA
	Max R_{BAT} voltage drop with R_{BAT} = 1k in low-power mode (V_{BAT} = 12V)	1.92V	1.75V	1.57V

The recommended range for the series resistor being attached to the supply pin BAT is 1 kΩ to 2 kΩ.

8. Series Resistor at Pin WAKE

As shown within the application diagram of the fault-tolerant transceivers, a series resistor in front of the pin WAKE is recommended in case an external switch to GND should be applied. Purpose of this resistor is to limit the current, if the control unit has lost its GND connection. This resistor is needed only in case the ECU might lose its GND connection (due to a contact failure) while the external wake-up source connected to the pin WAKE still is connected to GND.

In case of a GND loss on ECU level there is the possibility that the entire control unit becomes connected to GND via the external wake-up switch to an independent GND source (see also Figure 8). In order to limit the current in this special failure case a series resistor is required to protect the transceiver.

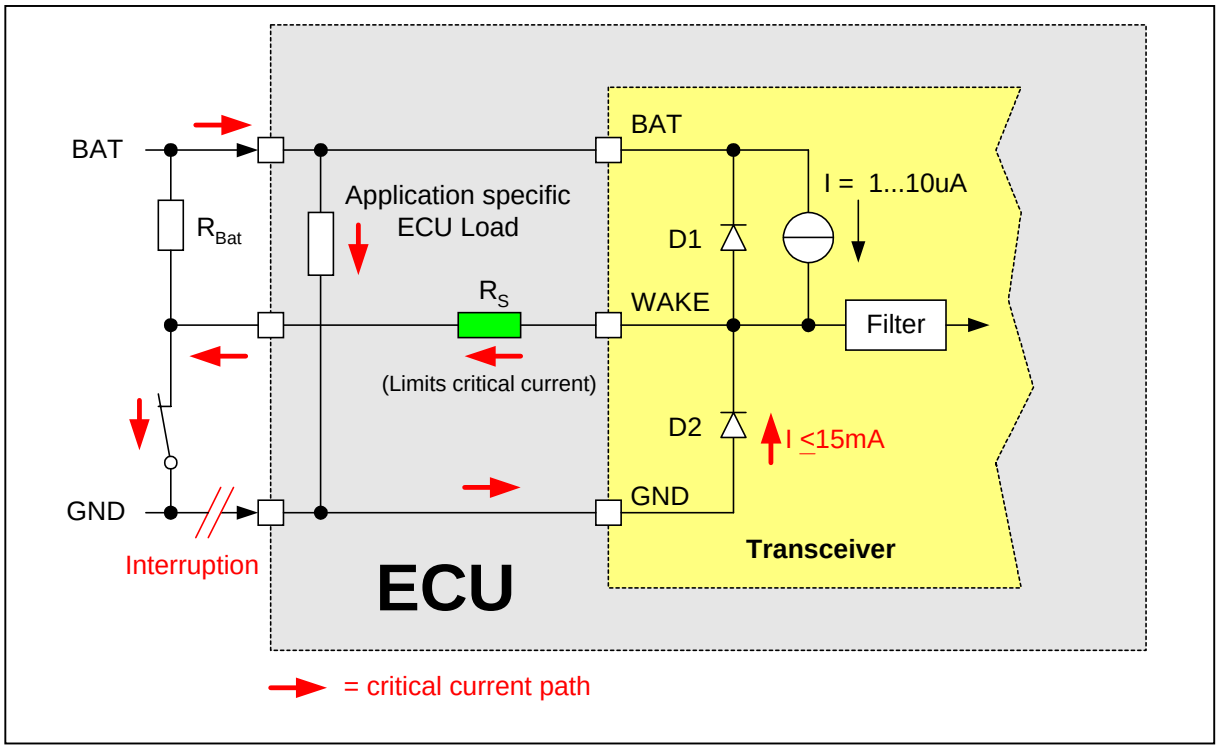


Figure 8 : Failure current path in case of "Loss of GND"

The pull-up resistor R_{Bat} shown within Figure 8 is used to guarantee a defined current within the external wake-up switch to GND in case it is closed. This current is needed to provide a good contact within the mechanical switch itself (contact corrosion …). The transceiver's integrated pull-up current source to BAT is not suitable to provide current for the application and used only to get a defined level at the pin WAKE in case of an open circuit condition.

8.1. Parameters defining the range of R_S

The value of the series resistor R_S connected to the pin WAKE is limited by following parameter :

- the maximum allowed current for the pin WAKE
- the input wake-up threshold voltage of the pin WAKE
- the internal pull-up current of the pin WAKE
- the maximum system GND offset between ECU and the external wake-up switch, which should be tolerated
- the maximum battery supply voltage

The maximum allowed current for the pin WAKE could be found within the “LIMITING VALUES” of the corresponding transceivers data sheet. The input threshold voltage and pull-up current for the pin WAKE can be found within the “DC Characteristics” section of the corresponding transceivers data sheet. The relevant values are collected within the following table :

Parameter	PCA82C252	TJA1053	TJA1054
Max input current I_{WAKE}	-15mA	-15mA	-15mA
Min input threshold $V_{th(WAKE)}$	1,2V	1,7V	2,5V
Max pull-up current I_{IL}	250uA	70uA	10uA

8.2. Calculating the limits of R_S

The maximum possible series resistor R_S is defined by the wake-up threshold of the pin WAKE, the GND shift between the ECU and the transceiver and the integrated pull-up current source of the pin WAKE. Following formula allows calculation of the maximum allowed series resistor :

$$V_{RSMAX} = V_{th(WAKE)MIN} - V_{GNDMAX}$$

$$R_{SMAX} = \frac{V_{RSMAX}}{I_{IL}} = \frac{\left(V_{th(WAKE)MIN} - V_{GNDMAX}\right)}{I_{IL}}$$

$$with V_{GND} = GND\ shift\ between\ Transceiver\ and\ wake-up\ switch$$

The minimum allowable series resistor R_S is defined by the maximum allowable input current for the pin WAKE. This maximum current must not be exceeded, even if VBat reaches its maximum voltage level. Thus the minimum series resistor R_S calculates as follows :

$$R_{SMIN} = \frac{V_{BatMAX}}{I_{WAKE}}$$

8.3. Example calculation

Assuming proper wake-up with 0,5V GND shift between the wake-up switch and the transceiver chip the maximum possible series resistor is calculated as follows (TJA1054) :

$$R_{SMAX} = \frac{\left(V_{th(WAKE)MIN} - V_{GNDMAX}\right)}{I_{IL}} = \frac{\left(2.5V - 0.5V\right)}{10uA} = 200kOhm$$

$$R_{SMIN} = \frac{V_{BatMAX}}{I_{WAKE}} = \frac{27V}{15mA} = 1.8kOhm$$

Parameter	Condition	PCA82C252	TJA1053	TJA1054
Maximum series resistor R_{SMAX}	0,5V GND shift	2,8k	17,1k	200k
Minimum series resistor R_{SMIN}	27V battery supply	1,8k	1,8k	1,8k

9. Series Resistor at Pin TXD

CAN protocol controllers typically provide relative strong output levels with fast signal slopes at their TXD output pins. These steep edges might cause some additional Electro Magnetic Emission (EME) on the CAN bus wires. In order to reduce this emission in the system, a series resistor R_{TXD} between the pin TXD of the CAN controller and the pin TXD of the transceiver is commonly used.
Because the transceivers are providing internal pull-up behaviour at the pin TXD, the range of the external series resistor is limited.

9.1. Parameters defining the range of R_{TXD}

Following parameter are limiting the external series resistor connected to the pin TXD :

- Maximum internal pull-up current of pin TXD ($I_{IL\ TXD\ MAX}$)
- Maximum dominant input threshold of the transceiver's pin TXD ($V_{IL\ TXD\ MAX}$)
- Dominant drive capability of the CAN Controller's pin TXD ($V_{DOM\ TXD\ MAX}$)

Parameter	PCA82C252	TJA1053	TJA1054
Max TXD input current $I_{IL\ TXD\ MAX}$	800uA	800uA	800uA
Max dominant input threshold $V_{IL\ TXD\ MAX}$	$0.3V_{CC}$	$0.3V_{CC}$	$0.3V_{CC}$

9.2. Calculating the Limits of R_{TXD}

The maximum possible series resistor within the TXD wire calculates as follows :

$$V_{R\ TXD\,MAX} = V_{IL\ TXD\,MIN} - V_{DOM\ TXD\,MAX}$$

$$V_{IL\,TXD\,MIN} = V_{CC\ MIN} \times 0.3$$

$$R_{TXD\,MAX} = \frac{V_{R\ TXD\,MAX}}{I_{IL\,TXD\,MAX}} = \frac{V_{CC\,MIN} \times 0.3 - V_{DOM\ TXD\,MAX}}{I_{IL\,TXD\,MAX}}$$

9.3. Example calculation

Assuming a minimum transceiver supply voltage of $V_{CC\ MIN}$ = 4.75V and a drive capability of the CAN controller with $V_{DOM\ TXD\ MAX}$ = 0.4V, the maximum series resistor allowed for the TXD connection between transceiver and CAN controller calculates as follows :

$$R_{TXD\,MAX} = \frac{V_{CC\,MIN} \times 0.3 - V_{DOM\ TXD\,MAX}}{I_{IL\,TXD\,MAX}} = \frac{4.75V \times 0.3 - 0.4V}{800uA} = 1.28kOhm$$

It has to be mentioned that any series resistor within the TXD connection increases the transmission delay of the system and thus has an impact to the timing conditions. It has to be checked individually, whether this additional delay is tolerated by the target application, especially if additional capacitance is connected to the pin TXD of the transceiver. The pin capacitance of the transceiver itself does not cause significant additional delay adding a series resistor of up to 1.28kOhm.

10. Hardware Design Checklist

The following table gives an overview about hardware issues to be checked for proper system design.

No.	Pin	Comment
1	VBAT	A series resistor of 1k ... 2k is recommended in order to increase the robustness against transients on VBAT (see also chapter 7).
2	VCC	Check proper buffering according to chapter 4.
3	RTH RTL	Check for proper system termination, total termination has to be about 100 Ohms, a single node's termination is recommended not to exceed approx. 6k. (see also page 26)
4	INH	INH is a VBAT related pin (open drain towards VBAT) and thus is **NOT** suitable to be connected directly to an input port of a microcontroller without external clamping or level adaptation.
5	WAKE	WAKE is a VBAT related pin (internal pull-up to VBAT) and thus is **NOT** suitable to be connected directly to a microcontroller port without external clamping or level adaptation.
6	WAKE	The output drive capability of the integrated pull-up to VBAT is intended to keep this pin on a defined level in case of an open circuit condition due to a failure on the PCB. This internal pull-up of some uA is **NOT** suitable to be driven directly by external circuitry like open collector bipolar transistors. The leakage current of such a transistor might be enough to cause a continuous LOW level at WAKE thus allowing no edges for wake-up anymore. An external default load or a push-pull driver is recommended here if this pin is used for local wake-up sources. (e.g. pull-up resistor to BAT ...)
7	WAKE	An unused pin WAKE is recommended not being left open due to immunity issues. Especially if some optional wiring is connected to this pin, this wire represents a potential antenna for environmental noise. Due to the integrated pull-up towards VBAT followed by an analogue filter, unwanted wake-up's are never observed for an open pin WAKE even with EMC load on it. Nevertheless it is recommended to connect an unused pin WAKE with the pin BAT of the transceiver for safety reasons. Pulling to VCC or GND is **NOT** suitable because this would result in a continuous current flow out of the internal pull-up to BAT.
8	WAKE	If the pin WAKE is directly connected to a wake-up source with separate GND connection (like an external switch to GND outside of the PCB) a series protection resistor is recommended as shown within the application diagram. This series resistor is used to limit the maximum current flowing in case the entire control unit has lost its GND connection. In this case, all the application current would flow through the external wake-up switch to GND. This may damage the transceiver. See also chapter 8, Series Resistor at Pin WAKE.

11. Software Design Hints

11.1. System Sleep Procedure

For a safe Sleep Mode transition of a system it is recommended to take care on possible wake-up events, which might occur in the same moment.

If the microcontroller drives the goto-sleep command to the transceiver, the pin INH gets floating after the “reaction time of the goto-sleep command” has been exceeded. Followed to this change at INH, the application’s voltage regulator typically gets disabled, VCC ramps down and the host microcontroller gets un-powered.
From system point of view it could happen, that the sleep process as described above gets interrupted by a wake-up event like a CAN message or an edge at the pin WAKE. As a result of this wake-up event, INH gets immediately HIGH again and VCC might keep stable all time due to the applied buffer capacitors. So the host microcontroller is continuously supplied without any power-on hardware reset even if it has performed the goto-sleep procedure assuming that VCC will go down now.

From software point of view, the application is recommended to check, whether the goto-sleep procedure was successfully finished or not, monitoring the pins RXD or ERR. RXD and ERR are providing the wake-up information during Goto Sleep and Sleep coding on STB and EN. So if ERR or RXD signals a LOW during the goto-sleep command, this is an indication that there was a wake-up event and VCC will keep active. Thus the software should react on this event as required by the application, e.g. restart the software (cold start).

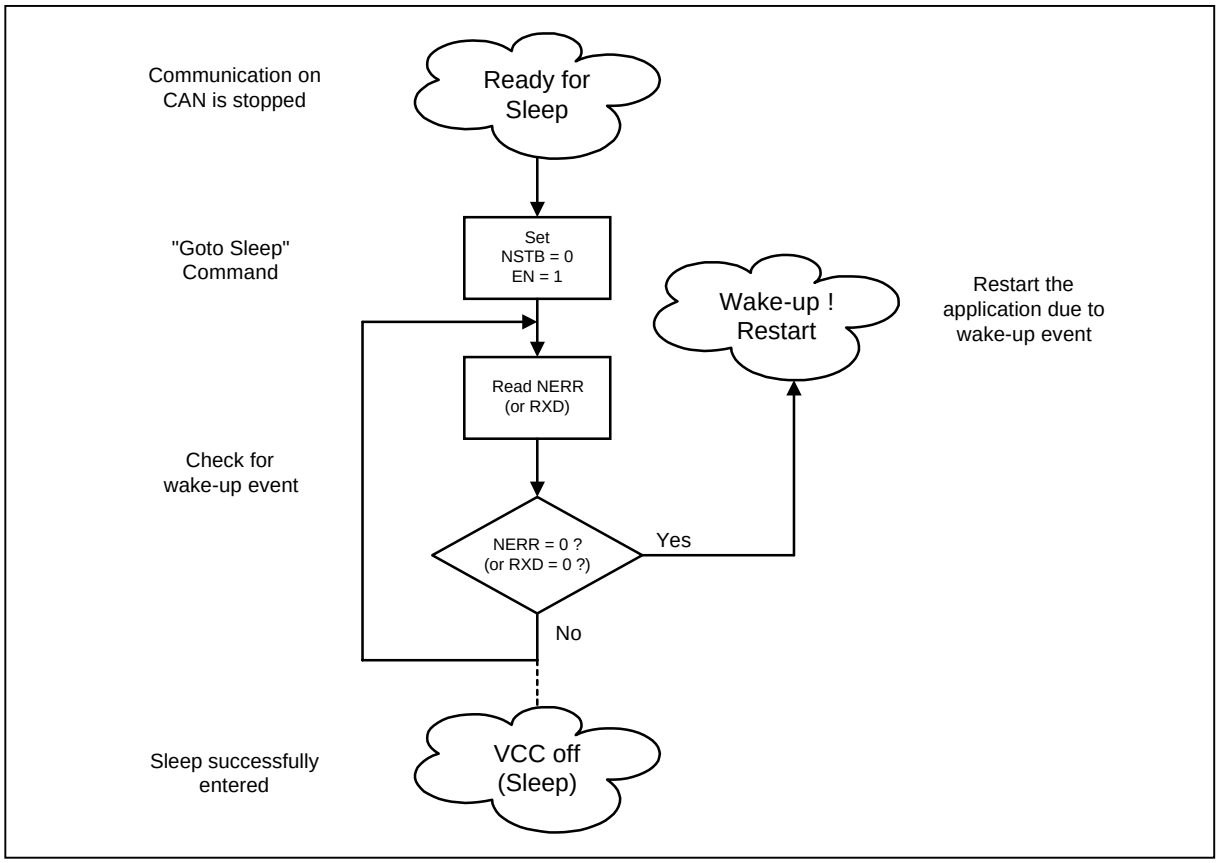


Figure 9 : Software Flow Example, Sleep Mode

11.2. Using the ERR output for failure diagnosis

During Normal Mode of the fault tolerant transceivers the pin ERR provides an active LOW information on detected bus failure conditions. In case of an error free physical medium, the pin ERR is set to HIGH level while any detected wiring failure results in a LOW output level. Depending on the physical failure condition, the ERR output behaves slightly different. Furthermore there is a slight difference between the devices concerning open wire failures as already mentioned within chapter 2.
Within an application, it is not recommended to route the ERR signal towards an interrupt input of the host microcontroller. Depending on the bus failure scenario, the pin ERR might toggle quite often resulting in an increased interrupt load to the controller. It is more common, reading the error information provided at the pin ERR from time to time within a CAN interrupt service routine.

11.2.1. ERR signal at open bus wires

In case one of the bus wires is opened due to a contact failure within the bus system, in a first glance this scenario is not visible to any of the transceivers. Both bus wires keep at their recessive level due to the distributed termination of the fault tolerant system and no transceiver will signal this failure situation.
As soon as a first node in the system starts transmitting a message, all nodes on the opposite side of the interruption recognise a missing bus signal on one of the wires. This missing signal is captured into the error flag (pin ERR) with a certain filter mechanism. All nodes located at the same side of the interruption like the sending node do not see a missing signal and thus do not signal an error condition. So depending on the location of the interruption, some nodes signal a problem while some other nodes do not signal this interruption. Since all nodes in the system will send out messages from time to time, the ERR output will toggle due to the fact that the failure is not visible for the sender as well as for the receivers on the same side of the interruption.

In order to achieve a better reliability of the ERR output signal, the transceiver implementations include a little failure counter, making sure that a single missing edge on one bus wire does not immediately toggle the ERR signal. Here the implementations differ slightly as shown within the following table :

Transceiver	Detection, ERR -> LOW	Recovery, ERR -> HIGH
PCA82C252 TJA1053	3 missing dominant edges on one of the bus wires	1 detected dominant edge on both wires
TJA1054	4 missing dominant edges on one of the bus wires	4 detected dominant edge on both wires

11.2.1.1.Behaviour using PCA82C252 / TJA1053

Systems using the PCA82C252 and the TJA1053 do not provide a stable ERR output signal after transmission of a message via a bus with interrupted bus wire. This is caused by the above shown failure recovery of these products. Assuming a node transmitting a message, all nodes on the other side of the interruption do signal a problem after 3 missing edges as desired. At the end of this telegram, all receiving nodes will write their acknowledge bit to the bus resulting in a proper dominant edge on both bus wires. So the ERR signal becomes cleared with the acknowledge bit at all nodes. Meanwhile the sending node of that message might see a single missing edge during the acknowledge period within the senders segment. But this single missing edge is not enough to pass the 3 missing edges counter. At the end of the message transfer, no node in the system will signal a bus failure condition even if the bus wire is interrupted. Thus no CAN interrupt service routine is able to detect this failure scenario using PCA82C252 and TJA1053 transceivers.
A hardware work around is connecting a capacitor of about 470nF between ERR an GND. This capacitor lengthens the LOW phase of the ERR output making it readable even within the CAN

interrupt service routine. The relative weak pull-up behaviour of ERR allows keeping the capacitor within this suitable range.

11.2.1.2.Behaviour using TJA1054

Within the TJA1054 this system problem has become solved with the new introduced failure recovery counter. The TJA1054 detects the open wire condition after 4 missing edges and recovers first with detection of 4 consecutive detected edges on both wires. Thus the single acknowledge bit coming from the receiving nodes is not sufficient to reset the detected failure condition and the ERR output keeps LOW all over the message frame length and further on into the next frame. With this optimisation, the capacitor useful for the PCA82C252 and TJA1053 designs becomes superfluous.

11.2.2. ERR signal while CANH shorted to GND or CANL shorted to VCC

In a first glance these two bus failure scenarios are again not visible to any of the nodes in the system because the bus levels do not change. The recessive bus level on CANH is already GND while CANL provides VCC as the recessive bus level. Thus these two shorts do not affect the recessive voltages on the bus.
As soon as one node starts a transmission, there will occur a missing bus signal on one of the bus wires. This corresponds to the behaviour of an interrupted bus wire with the difference that all nodes in the system will detect this missing single wire bus signal including the sending node. Thus there is a global detection and signalling of that problem all time.
If these shorts are removed from the bus wires, the ERR signal keeps present, because the internal “missing edge counters” are still overflowed. If now the first message is transmitted after removing the bus failure condition, the edges of this message clear the error signal present at the pin ERR depending on the implemented recovery counter. The TJA1053 and PCA82C252 will recover with the first dominant edge while the TJA1054 will recover with the 4^{th} detected dominant edge.

It should be noted that common mode chokes used within a fault tolerant system might corrupt the proper failure signalling, depending on the location of the short compared to the sending node. The chokes try to force symmetrical signals on the physical medium, which is not possible due to the present short circuit. Nevertheless due to the choke’s inductance there is a significant cross coupling between the unaffected bus wire and the shorted bus wire, especially within bus segments far away from the short circuit. This cross coupling could become that high that the shorted bus wire carries enough signals to bypass the “missing edge counters”. So it might happen, that the short circuit condition is not signalled very stable all over the network. Removing the common mode chokes from the network solves that phenomenon.

11.2.3. ERR signal while other short circuit conditions

All other bus short circuits are influencing the recessive bus levels directly and thus could be detected by the transceivers without the need of bus traffic. If the bus levels deviate from the nominal levels for a certain time frame, this condition is detected and signalled directly at the pin ERR with an active LOW signal. Upon recovery from these shorts, ERR gets high again.
It should be noticed that the “missing edge counter” is still operating in the background and possibly overflows due to missing single wire signals during communication. In fact there is a double detection of the failure situation. Thus recovery from a directly detected short circuit might take place with the next couple of successfully detected edges first. Therefore the pin ERR does not immediately fall back to HIGH if the short is removed from the bus. Again some bus communication with proper edges on both bus wires is needed to recover the ERR signal to HIGH.

11.3. Using ERR for Reading out the PWON Flag

The so-called Power-on Standby Mode offers reading out the internal PWON Flag of the fault tolerant transceivers. Setting the control pins STB and EN accordingly results in switching the pin ERR immediately to the internal PWON flag. Nevertheless this takes some gate transition times before the PWON flag gets visible at the pin ERR. This switching time is mainly influenced by the external load condition present on the pin ERR. Since the High-side output drive capability of this pin is limited, a significant time is needed before the application controller could read the desired value.

Example :
Assuming a typical pin load of about 20pF caused by the PCB and the connected microcontroller the time constant for a LOW to HIGH transition on the pin ERR would calculate as follows :

$$t_{LOW->HIGH} = \frac{0.9V}{100uA} \times 20\,pF = 180ns$$

$$with\ \ 0.9V = drop\ of\ \ ERR\ driver\ @\ 100uA$$

This switching time might be that long that an application software reads the pin ERR information too early after setting the corresponding mode via STB and EN. Thus software designers should take care in the above mentioned charge times at ERR and implement a suitable waiting time between selection of the mode and reading out the ERR signal.

The signal HIGH to LOW transition is much faster due to the low-side drive capability of the pin ERR. Thus here is no timing problem expected.

$$t_{HIGH->LOW} = \frac{0.4V}{1.6mA} \times 20\,pF = 5ns$$

$$with\ \ 0.4V = drop\ of\ \ ERR\ driver\ @\ 1.6mA$$

12. Frequently Asked Questions

12.1. The transceiver does not enter the Sleep Mode

- The TJA1054 needs to be set into Normal Mode once after first battery connection, the TJA1053 does not. For compatibility reasons the software should set the transceiver into Normal Mode whenever a power-on condition was detected (e.g. by reading the PWON bit during PWON Standby Mode)
- The so-called "goto-sleep command" was driven too short by the uC. This command has to keep active for at least 50us (STB=0, EN=1) in order to make sure that it is accepted by the transceiver. The value could be found within the data sheet located at the timing characteristics : “minimum hold time of goto-sleep command” (PCA82C252 and TJA1053) / “reaction time of goto-sleep command” (TJA1054).
- There was a wake-up event during the “Goto Sleep” procedure. (see also 11.1.)
- The pin WAKE is connected to the local 5V supply, which is controlled by the pin INH of the transceiver. In this case the Sleep Mode was entered successfully and the pin INH becomes floating. As a result of this the 5V supply is switched off -> VCC drops down. These forces an edge at WAKE and the device wakes up again. If WAKE is not used within the application it should be connected directly to the pin BAT of the transceiver.
- There is an external CAN-Tool connected to the network and the GND connection between the PC and the application is missing. The floating bus wires are forcing wake-up events for the application.
- The GND connection between separate powered nodes is lost. Result as discussed above.

12.2. System operates in Single Wire Mode all time

- There is still a termination resistor between the bus wires present as known from the high-speed physical layer. E.g. a CAN tool with high-speed transceiver and termination is connected. The fault tolerant physical layer has **NO** termination resistor between the wires but a distributed termination at all nodes connected between pins CANH and RTH, CANL and RTL. See also chapter 5.

12.3. System does not wake-up, even if there is bus activity

- For bus wake-up a CAN message with 5 consecutive dominant bits is required. This guarantees the minimum dominant time of 38us needed to wake-up the transceiver. Depending on the bit rate even messages with less than 5 consecutive dominant bits are sufficient to achieve the 38us dominant requirement.
- Systems using the Standby Mode keeping the VCC supply alive are usually waked up with a dominant edge at RXD or ERR respectively. Depending on the uC hardware and software, this edge might be lost for the uC with the result that the uC enters its low-power mode (Stop Mode) with RXD and ERR continuously set LOW (wake-up). There are no further edges and thus the uC does not wake up. For these applications it is recommended to support a level sensitive wake-up or to make sure that all edges are recognized independently from software actions.

12.4. Transceiver is damaged when external tools are connected

- Since PC's and other external equipment is typically supplied from the AC power supply while the car is isolated and supplied from a battery, there might be a very high voltage difference between both CAN networks. It is recommended to make sure that the GND line between external stuff and the car is connected first, followed by the bus lines in order to have the same reference level.

12.5. CAN tool cannot communicate with certain application

- Often a CAN tool is used to simulate the entire car environment for functional verifications of a single application. The problem is that the CAN tool does not provide the same termination resistance as present in the car's environment. In order to get this set-up running the CAN tool has to be supplied with a lower internal termination. It is recommended to replace the existing resistors inside of the CAN tool with e.g. 500 Ohms (the minimum allowed termination per transceiver) for test purposes. The total termination of all nodes should still keep above or equal to 100 Ohms.

12.6. No communication at CANH to VCC short circuit

- There is a TJA1053 or PCA82C252 transceiver within the network. These products do not support the short circuit "CANH to VCC". The TJA1054 is the first transceiver tolerating these short circuit conditions. Please check all connected hardware on presence of these transceivers, especially within connected CAN PC-tools.